Announcement of MOSIS MPW Sponsorship Through Intel Custom Foundry

The University of Southern California's Information Sciences Institute operates MOSIS (Metal Oxide Semiconductor Implementation Service), to provide metal–oxide–semiconductor (MOS) chip design tools and related services that enable universities, government agencies, research institutes and businesses to prototype chips efficiently and cost-effectively. The MOSIS Service, is collaborating with Intel Corporation to provide access to 22nm FinFET Low-power (22FFL) process technology for the microelectronics design community through the Intel Custom Foundry. To encourage participation in the MOSIS Service offerings of Intel's multi-project wafer (MPW) fabrication runs, the Office of the Under Secretary of Defense for Research and Engineering (OUSD(R&E)) Trusted and Assured Microelectronics (T&AM) Program aims to potentially sponsor MPW runs in government fiscal year (GFY)-2020 and GFY-2021. Projects aligning with the R&E Microelectronics Roadmap's need for access to State-Of-The-Art (SOTA) technology will be considered for subsidized fabrication if those designs and/or design efforts are complementary to the T&AM objectives of enhancing the U.S. microelectronics development capability.

This represents a significant opportunity to obtain access to cutting-edge microelectronics from a U.S. domestic foundry through MPW fabrication. Key objectives of the OUSD(R&E) T&AM program include enhancing the U.S. microelectronics ecosystem, providing access to a rich set of intellectual property (IP), utilizing next-generation secure design methodologies, and creating a highly-trained workforce. These objectives require regular access to state-of-the-art (SOTA) semiconductor technologies by commercial entities, the defense industrial base, and U.S. academic researchers. This announcement aims to inform the U.S. microelectronics community of an opportunity for SOTA access and to identify interest in participating in MPW runs in GFY-2020 and GFY-2021.

For an in-depth understanding of Intel's 22nm FFL process technology, the users are referred to the following publications: "*22FFL: A High Performance and Ultra Low Power FinFET Technology for Mobile and RF Applications*" (IEEE IEDM 17-685), and "*Intel 22nm FinFET (22FFL) Process Technology for RF and mmWave Applications and Circuit Design Optimization for FinFET Technology*" (IEEE IEDM18-316) written by Intel's staff.

To be considered for participation in a GFY 2020 MPW run, please submit a request for sponsorship. This request should be a pdf file attached to an email addressed to Dr. Devanand Shenoy, 703-812-3708, dshenoy@isi.edu, and to Dr. John N. Damoulakis, 703-812-3718, jdamoulakis@isi.edu. The request should not exceed one page, it should be unclassified, and should not contain any proprietary information. The request should provide the following information:

- Clearly identify the requesting organization (limited to U.S. Companies and Universities).
- Identify the organization creating the chip design.
- Identify the expected use of the fabricated chip(s).
- Identify the IP needed for riding the 22FFL MPW seat, as well as the approximate area of the fabricated chip(s).

- Identify the potential added value/functionality from using Intel Custom Foundry.
- Identify the value to the U.S. Government or the research community from receiving this sponsorship.

Please submit your Request for Sponsorship not later than February 28, 2020.