Electromagnetic Warfare (EW) Projects

Gallium Nitride (GaN) Amplifier Prototypes Targeting Microwave to Submillimeter-wave Frequency Spectrum (GaNAmp) - $16.2M, Lead: CA DREAMS – University of Southern California (USC) and Northrop Grumman-

California Defense Ready Electronics and Microdevices Superhub (CA DREAMS) Gallium Nitride Amplifier Prototypes Project (GaNAmp) aims to mature advanced gallium nitride (GaN) technology to enable broad-spectrum, high power, and high efficiency solutions for future DoD EW systems. The project will develop GaN amplifier chipsets from the microwave to the sub-millimeter wave frequency spectrum making advancements at the semiconductor-device, the integrated circuit, and the package level. Currently, GaN advancements occurring in labs are not transitioning fast enough to DoD applications. U.S. access to GaN technology above a technical readiness level/manufacturing readiness level (TRL/MRL) 5 level of maturity is limited to few onshore foundries and prototyping cycles are on the order of multiple-years for device, IC and packaged-solution-for EW electronics. On this CA DREAMS project, we plan to leverage university advancements for foundational material (UCLA/UCSB). Advance GaN TRL/MRL in 4 foundries (NG, HRL, Teledyne, Transphorm/Monde) and leverage innovative packaging approaches to accelerate prototyping cycles – with the goal that design IP be leveraged at the next-higher assembly for DoD EW applications. By exercising the CA DREAMS operational model, GaNAmp will demonstrate an increase in TRL/MRL of on-shore GaN foundries, demonstrate a 2x reduction in prototyping time cycles in the first year of the program, and demonstrate an increase in packaged V-band, and W-band RF) power capability.

Co-packaged Reconfigurable Signal and Intelligence Architecture (CORSAIR) - $8.6M, Lead: Midwest Microelectronics Consortium hub (MMEC)-Lockheed Martin-

The Co-packaged Reconfigurable Signal and Intelligence Architecture (CORSAIR) project seeks to provide an Electromagnetic Warfare (EW) solution for a multi-chip package with high-speed data converters and in-line accelerators. Current EW systems require nearly unlimited adaptability and unique analysis routines which ideally switch at waveform speeds and are paired with dense, low-latency compute resources. Today's EW system performance and adaptability are limited by Size, Weight, Power, and Cost (SWaP-C). Power and latency-efficient systems such as ASICs and CPUs are largely static and cannot change functionality dynamically while programmable systems such as Field Programmable Gate Arrays (FPGAs) and Graphical Processing Units (GPUs) don't meet power and latency requirements. Current EW solutions remain inflexible and achieve limited adaptability. CORSAIR will develop a fully programmable, RF-enabled dual-use chiplet targeting >20x system-level performance versus incumbent technology in signal processing. The CORSAIR chiplet will also enable artificial intelligence (AI) in the same silicon without excessive tuning or specificity. CORSAIR is built on Intel's dual-use, 18A-based Configurable Spatial Architecture (CSA). The project will deliver a prototype multi-chip package (MCP) integrating a domestically produced CSA chiplet with an Intel Agilex 9 direct

RF drive device to deliver a wideband, rapidly reconfiguration RF processing device. CSA executes dataflow. This data flow is a general, explicitly parallel architectural paradigm in which programs are represented as graphs. In the dataflow paradigm, vertices are computation and edges are data communications. The CSA executes static dataflow graphs derived from C/C++ programs which are configured onto the array prior to execution, establishing dedicated paths between the array of arithmetic logic units (ALUs). CSA implements dataflow as a dense, energy-efficient spatial array comprised of thousands of ALUs connected by a routing network. Once configured, CSA computes like a fixed-function pipeline with minimized switching in the chiplet fabric. The coupling of dataflow architecture and spatial microarchitecture fundamentally improves all silicon and programmability metrics versus currently deployed runtime reconfigurable array architectures (RTRA). The CORSAIR prototype performance and reconfigurability are expected to transform the art-of-possible in spectrum sensing. Modeling has shown an average processing gain of 16 decibels (dB) relative to conventional iso-process FPGA and 20dB of gain in estimated EW signal processing applications achieving sub-100 nanosecond (ns) switching latency through a combination of a high-performance memory systems, a small program file, and specialized execution and caching techniques enabled by dataflow. The CORSAIR effort is led by Lockheed Martin working in partnership with Intel. LM will provide hardware and software design support for the dual-use, 18A-based processor. Intel will provide device design, performance simulation, emulation, fabrication, prototype packaging, testing, and evaluation support. The CORSAIR prototype MCP performance will be evaluated by the Sensors Directorate at the Air Force Research Laboratory (AFRL/RY). This project is expected to mature the CSA components from a TRL/MRL of 4 to a capability to produce prototypes in a production environment (MRL 6/7).

a giant Leap AheaD for all filter DesignERs! (LADDER) - $4M, Lead: Northeast Microelectronics Coalition hub (NEMC)-Akoustis-

The LADDER project aims to create a bulk acoustic wave (BAW) filter synthesis tool, enabling those broadly trained in electrical engineering, and without specific training in BAW filter design, to rapidly design a filter to a set of linear and non-linear specifications. Currently, BAW filters are designed by highly trained specialists executing painstaking optimization using microwave circuit simulators, layout tools, and finite-element modeling (FEM). The design process is manual, complex, iterative and time-consuming. Project lead, Akoustis, will develop LADDER. Filter performance on par with current best practice will be achieved by replacing the manual, complex, and iterative process with an automated intelligent algorithm which can, over time, leverage the power of AI/machine learning (ML) to learn the "art" of filter design. LADDER is projected to reduce RF filter design time from man-months to machine-days and machine-hours. LADDER will enable the broad adoption of BAW filters in DoD system by efficient utilization of Akoustis' XBAW® and XP3F foundry manufacturing services, thus enabling miniaturization of DoD RF system hardware and increasing functionality and performance. Project partners AFRL, Army Research Lab (ARL) and Raytheon Technologies) will design RF filters by both traditional methods and LADDER and compare simulated and measured filter performance. Akoustis will manufacture filters designed by both traditional methods and LADDER at S, C and X-bands. Project partner University of Pennsylvania will enhance the filter process design kit (PDK) by characterization and development of non-linear resonator models. Ultimately, LADDER will enable the U.S. defense industrial base (DIB) and Microelectronics Commons (Commons) community to rapidly design high-performance filters from S to Ku-band.

Heterogeneously Integrated Tunable High-Q X-Band Acoustic Filters for Electronic Warfare (HITFEW) - $1.8M, Lead: Air Force Research Lab (AFRL)-

This project seeks to improve the state-of-the-art (SOTA) in terms of size and performance for chip scale acoustic RF filtering technology to accommodate the future projected needs for RF sensors in DoD across all domains in the context of the current and future electronic warfare environment. The effort will result in working prototypes using advanced microscale integration methods of fixed and tunable filters in the X-band targeting element level front end electronics for active electronically scanned array (AESA) radars and co-site interference autonomous cancellation systems for electronic support measure receivers. Methods for packaging and integrating these components will occur along with the advancement of the components themselves.

Workforce Enhancement Specializing in Advanced Packaging and Heterogeneous Integration (WEAVE-HI)- $0.80M Lead: AFRL-

This project has funded two additional on-site contractors over 24 months to develop advanced packaging solutions in the AFRL Sensors Directorate packaging lab for power dense transistors and diodes prototyped in government laboratories. The packaging laboratory holds significant capability to enhance the state of microelectronics research through engineering novel packaging strategies which increase thermal stability, heat dissipation, chip density, and integration complexity. This enhancement of the advanced packaging workforce has built in-house skills and avoided technology leakage in a critical part of the microelectronics ecosystem. The new employees have been successfully trained and integrated into the team and have created significant value through hands-on research. In December 2024, the hires implemented the 2.5D heterogeneous integration process, Metal Embedded Chip Assembly (MECA), on thermally limited Ga2O3 Transistors resulting in a 40% decrease in transistor operating temperature. This will enable high power densities while maintaining mean time to failure for next generation power electronics technology.

3D Interposer Technology -$1.15M Lead: Army Research Lab (ARL) (3DINT)-

The objective of this effort is to develop and demonstrate 3D interposer technology based on additive manufacturing for high density electronics. The interposer is the key for custom DoD packaging of commercial electronic chips and chiplets, and is needed for tightly integrated, small, and efficient products. This project will develop the 2-photon polymer (2PP) additive manufacturing technology, together with pyrolysis and electroplating, to rapidly fabricate 3D interposers with integrated thermal management for DoD applications.

Wideband Same-Frequency STAR Array Platform Based on Heterogeneous Multi-Domain Self-Interference Cancellation (SF STAR) - $5.6M, Lead: NEMC-Sivers Semiconductors-

The project aims to develop RF and baseband cancellers and digital cancellation algorithms and prototype them in a STAR array platform. Existing Navy and Marine Corps systems cannot simultaneously support multiple functions with a single integrated device. More specifically, radar networks cannot communicate with other node locations and/or perform additional functions, such as electronic support measures (ESM), when the radar is active. Conventional RF systems either transmit and receive at different time slots or at different frequencies. To optimally use the available bandwidth, it is highly desirable to be able to transmit and receive at the same time on the same frequency. This capability is usually called same-frequency simultaneous transmit and receive (SF-STAR). STAR systems eliminate reliance on rigid spectrum allocations and enable multifunction operation, rapid deployment, and better ability to react and respond to a changing electromagnetic environment. The program aims to advance the TRL of SF-STAR phased arrays with a demonstration of tactically relevant capabilities. We are constructing a subsystem testbed comprising a fully digital phased array based on technology breakthroughs on previously internally funded programs at Massachusetts Institute of Technology-Lincoln Lab (MIT-LL). BAE Systems has significant prior experience developing wideband, high-linearity RF-domain self-interference canceller systems. We bring to this effort a TRL-4/MRL-6 solution, which is currently designed for a lower frequency range than what we are proposing for this project. Columbia has a long history of developing complementary metal oxide semiconductor (CMOS)-based high-degrees-of-freedom cancellers for STAR applications, using frequency-domain and time-domain architectures under the DARPA RF-FPGA, SPAR, and WARP programs.

High-Performance Diamond Electronics for Next Generation Defense Systems (HPDEW) - $6.2M, Lead: Silicon Crossroads Microelectronics Commons hub (SCMC) -Great Lakes Crystal Technologies-

Today’s state of the art high power RF and power transistors for electromagnetic warfare systems are based on silicon carbide (SiC) and gallium nitride (GaN), respectively, both of which are wide bandgap (WBG) semiconductors (WBG) that have superior properties compared to previous generation semiconductors that included silicon (Si) and gallium arsenide (GaAs). The use of WBG semiconductors translates to the ability to handle higher power densities, faster switching times, smaller form factors, lower switching losses, and overall higher electrical efficiency. While very successful, these WBGS are reaching their ceiling, in large part due to thermal power dissipation limits. Furthermore, it is becoming increasingly clear that future drones, electric vehicles, and all-electric ships will require higher performance RF and power electronics than what can currently be achieved with SiC or GaN. This project seeks to develop TRL-5, MRL-5 diamond-based electronics that expand sensing capability overmatch by providing superior power densities based on diamond’s disruptive advantages of higher breakdown electric field and higher thermal conductivity. The desired end-state includes technology maturation of a new class of diamond microelectronics for RF and power electronics applications. The HPDEW project leverages multiple SCMC functions and benefits. To support HPDEW development efforts, GLCT acquired relevant EDA tools via SCMC-supported EDA Access. Also, as a part of the RF characterization and testing portion of this project, GLCT is leveraging SCMC-funded infrastructure

implemented at the University of Notre Dame. Finally, and most impactfully, through SCMC external engagement and alignment, GCLT has received an additional $2.7m in supplemental funding from the National Security Innovation Capital (NSIC) efforts under the Defense Innovation Unit (DIU) to scale volume production of these diamond-based electronics to support current and future

Electronic-Photonic Integrated Circuits (ICs) for BEAM Steering (EPIC-BEAMS) - $2.9M, EW, Lead: ARL-

This Fiscal Year (FY) 2025-2026 effort will demonstrate RF and optical links and beam steering systems using Photonic Integrated Circuits (PICs). The effort leverages capabilities and components to be created in our FY 2023 Commons effort as well as existing non-Commons efforts. These PICs will be fabricated and packaged at the Office of the Under Secretary of Defense for Research and Engineering's (OUSD(R&E)) American Institute for Manufacturing Integrated Photonics (AIM Photonics) (also a member of the NORDTECH). Additional components and subsystems will be designed and characterized, including integration of peripheral electronics and active optical materials for EW.

Electronic-Photonic ICs for BEAM Steering (EPIC-BEAMS)- $1.40M Lead: ARL-

This FY 2025-2026 effort will demonstrate RF and optical links and beam steering systems using PICs. The effort leverages capabilities and components to be created in our FY 2023 Commons effort as well as existing non-Commons efforts. These PICs will be fabricated and packaged at the OUSD(R&E)'s AIM Photonics (also a member of the NORDTECH). Additional components and subsystems will be designed and characterized, including integration of peripheral electronics and active optical materials for EW.

Center for Technology Transition and Rapid Prototyping of Infrared Detectors (CENTROID) - $8.8M, Lead: MMEC-The Ohio State University-

The Center for Technology Transition and Rapid Prototyping of Infrared Detectors (CENTROID) project seeks to provide an EW solution for advanced integration of electro-optic and infrared (EO/IR) with microelectronics. Very large-format focal plane arrays (FPAs) are a valuable and necessary component to the growing sensor shield surrounding our warfighters with protection and situational awareness. The current SOTA uses single-chip stitched CMOS Digital Read Out Integrated Circuit (DROIC) to underpin these large FPAs. However, these DROICs become more difficult and expensive to produce as their size grows, mainly due to manufacturing yield loss. For some of the largest FPAs, it may take 20 or 30 wafers to yield each DROIC die and then it may take five DROIC die or more to yield one FPA. Consequently, a single yielded FPA may require more than 150 CMOS foundry wafers to produce. This yield loss drives the schedule, risk, and cost of large-format FPAs making it prohibitive to proliferate such solutions into a broader range of applications. The CENTROID project will develop cost-effective advanced large-format 3D infrared focal plane arrays (IRFPAs) by integrating pre-screened high-yield DROIC chiplets with seamless large infrared sensor array via a high-yield, high aspect-ratio interposer wafer. CENTROID will prototype a broad-band midwave-infrared (MWIR) detector with a nominal 4k x 4k resolution and a 10 µm pixel pitch. CENTROID revolves around two closely collaborative and interactive "lab to fab" loops to address the technical challenges for manufacturing high resolution large-format FPAs. The Technology

Transition loop will leverage advanced microelectronics 2.5D/3D heterogeneous integration and develop revolutionary methods to fabricate high resolution, large-format IRFPAs at higher yield, higher throughput, and lower cost than the state-of-the-art technology. The Rapid Prototyping loop will develop advanced detector capabilities that can be inserted into the Technology Transition loop's products for ultimate sensor performance to meet the overall goals of the DoD. Rapid Prototyping efforts will focus on investigation of modulation transfer function (MTF) in bulk and superlattice material for ultra-small pitch MWIR FPAs and heterostructure engineering of the detector architecture to minimize lateral diffusion. At small pixel pitch, the MTF can degrade due to lateral carrier diffusion. Novel bulk and superlattice heterostructure detector materials will be grown and characterized. Impact of dual-band (SWIR/MWIR) detector architectures and small pitch FPAs on the MTF and other radiometric parameters including noise equivalent temperature difference and spectral cross-talk will also be examined. The results of these studies and the improved device structures will be shared with the Technology Transition loop for integration into the overall structure. The objective of the Technology Transition loop is to solve the low yield constraint of large-format infrared sensors. This will be done by separating the complex DROIC circuitry into high-yielding and low-cost chiplets which will be yield-tested prior to integration. These Known Good Die (KGD) DROIC chiplets will then be reconstituted into a wafer that will enable wafer-scale hybridization. Critical processes needed for successful wafer-scale processing including through silicon vias (TSVs) in the interposer wafer will be refined to support scale fabrication. The MMEC is acting as Prime for the CENTROID project providing program management and coordinating activities among the technical performers. These performers include: 1) The Ohio State University which will be focusing on IR detector material growth and characterization, 2) SK Infrared which will be responsible for detector design, fabrication and testing, 3) Senseeker Engineering which will be working DROIC and interposer design, development, and characterization and 4) Attollo Engineering which performs detector wafer processing, 3D heterogeneous integration and final testing of FPAs. NSWC Crane will provide independent assessment of component technologies. Several of the technologies in CENTROID are starting at a relatively low TRL/MRL level of 2/3 but the end state of the fully integrated prototype is expected to be TRL/MRL of 5/6.

Tri-Band Infrared Focal Plane Array for Threat Warning and Long Range Fire Capabilities (3IRFPA) - $2M, Lead: AFRL-

This project seeks to demonstrate a three-color infrared image sensor that will enable multi-function operations (e.g. detect, track, and identify threats). This will be accomplished by stacking detector bands using a novel 3D heterogeneous integration technique that allows each band to be individually grown and stacked between optical filters. The final product will be tri-band focal plane array(s) (FPAs) on a digital readout integrated circuit (ROIC) with test electronics and dewar that comprise a fully functional prototype camera